REMARKS

Applicants respectfully request reconsideration of this application, as amended.

Without concession as to the propriety of the outstanding rejections, the claims have generally been amended for clarity and consistency. Additionally, claims 22 and 32 have been cancelled.

Amended claim 20 recites, *inter alia*, determining a specific condition for the integrity of a datum of said information to be transmitted on said data bus, reading the processing device of said datum transmitted from the storage device to the processing device on said data bus, processing said datum and executing a logic verification operation on all bits of said datum which is transmitted on said data bus, by the processing device or by the means for checking the integrity of information, during the processing for verifying that said specific condition is satisfied and disabling the processing device if a specific condition is not satisfied. Support for these amendments can be at least found on pages 3, 4 and 5 of the specification.

The Office Action asserts that Holtey discloses a method which comprises selecting a piece of sensitive information stored in the storage device, determining a specific condition for the integrity of the information, reading, by the processing device, of said information transmitted from the storage device to the processing device for processing via a data bus, processing the information and verifying by the processing device during processing that the specific condition is satisfied and disabling processing of the information if the specific condition is not satisfied.

Applicants respectfully submit that Holtey is directed toward a security access control unit which performs a key validation operation for a protected block by serially comparing the bits of a key value against the bit contents of lock bit positions of the

memory read out in response to such instructions. Holtey states on Column 3, lines 5-8 that the chip memory is organized into a number of blocks, each block having a number of rows, each containing a plurality of addressable byte locations. Each row further includes a single lock bit location. As a consequence, Applicants respectfully submit there is no teaching or suggestion in Holtey of any logic verification operation being applied to all bits of said datum transmitted on said data bus. Holtey also fails to teach or suggest the detection of the alteration of any bit of datum transmitted on a bus. In contrast, the disclosure of Holtey relates to the detection of the alteration of a single block bit. The plurality of bit memories in Holtey are reserved for security.

In that claim 20 relates to processing the datum and executing a logic verification operation on all bits of the datum which is transmitted on said data bus all data bits are secure. Thus, in that claim 20 contains features not taught or suggested by Holtey, Applicants respectfully submit the claim is patentably distinguishable therefrom.

Regarding claim 21, Holtey teachs on Column 3, line 24 comparing the bits of a key value against the bit contents of lock bit positions of the memory block read. However, Holtey fails to teach or suggest the detection of an alteration of an operation coder read in memory.

Regarding claim 23, Holtey fails to teach the use of logic operators at one different end of the data bus.

In relation to new claim 39, the claim recites that both logic operators are parity generators each having two logic opposite outputs and one logic selection input determining the one of the both logic outputs which is input in the comparator.

Support for this claim can at least be found on page 7, lines 4-6 of the specification and page 9. Applicants respectfully submit that there is no teaching or suggestion of parity generators being used as logic operators in Holtey.

Regarding the various rejections under 35 U.S.C. §103, Applicants respectfully submit that the alleged combination of Geronimi, Anderson and Takahira is untenable. First, Anderson is directed toward methods of attacks on tamper resistant devices wherein Geronimi and Takahira are directed toward protection systems. Anderson specifically states on page 2, paragraph 4, that it is directed toward techniques that can make smartcards and other devices vulnerable to attackers. As a consequence, the teachings of Anderson would not be combined by one of ordinary skill in the art with the protection systems of Geronimi and Takahira.

In general, Geronimi teaches a register whose inputs are connected to various security sensors. On Column 2, lines 18-22, Geronimi says that the register is tested first before each transmission of information to the exterior of the integrated circuit and second, before each modification of information in memory. However, Geronimi fails to teach detecting alteration of all bits of a datum on the bus which transmits information.

The passage of Takahira relied on by the Office relates to means for performing error checking and means for producing an error check code. However, as specified on Column 3, lines 5-12 of Takahira, a protected block is taught which cannot be accessed by a connected terminal. The protected block is adapted to store identification data and error check code associated with an application block. Takahira also specifies that a step is performed on the data group resident in the application file block, by the detecting error on the data in the file. The content of a determined application block is examined in association with a determined protected block. However, Takahira fails to teach detecting

alteration of all bits of a datum transmitted on a bus and to the contrary, in Takahira, error check code is recorded in a memory location in the protected area.

Regarding claim 21, amended claim 21 recites wherein said information datum is an operation code datum read in the storage device, all of the types of said operation code datum being contained in a table having a content determined during the manufacture of the security module, and the specific condition for the integrity of the information being said operation code datum is equal to a valid operation code datum of the table and at least operation code data composed by bits all equal to a same binary value are non-valid operation code data of the table. Applicants respectfully submit that there is no teaching or suggestion in Geronimi of enabling checking instruction data during the transmission on a bus.

Amended claim 23, relates to a first and second logic operator disposed at each one different end of the data bus. Applicants respectfully submit the combination of features is not rendered obvious or anticipated by Takahira which does not enable checking instruction data during the transmission on a bus.

Accordingly, with all claims being patentably distinguishable from the cited references, taken either alone or in combination, the outstanding rejections are untenable and should be withdrawn. A Notice of Allowance is respectfully requested.

Should the Examiner believe that any further action is necessary to place this application in better form for allowance, the Examiner is invited to contact Applicants' representative at the telephone number listed below.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (T2146-906833) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is

required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

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By: _____
Edward J. Kondracki
Reg. No. 20,604

Jason H. Vick
Reg. No. 45,285

Miles & Stockbridge, P.C.
1751 Pinnacle Drive
Suite 500
McLean, Virginia 22102-3833
(703) 903-9000

#9305201